Remarks

Office Action dated December 1, 2003 rejects claims 1-5, 8-11, 14, 16, 18, 21, 23, and 26 and objects to claims 6, 7, 12, 13, 15, 17, 19, 20, 22 and 24. In response, claims 1-24 remain unamended and claim 26 is cancelled. Consideration of the following arguments in favor of patentability is respectfully requested.

Claim 1 is rejected as anticipated by U.S. Pat. No. 6,094,733 to Momohara (herein "the Momohara patent"). In response, claim 1 remains unamended. The Momohara patent is directed to a semiconductor tester that performs a test on a device ("the DUT"). See col. 7, lines 3-8. Data is stored in the event of an abnormal reading. The data is later used for conditional execution of a process for replacement of defective memory cells with spare cells. See col. 7, lines 15-20. In order to decrease test time, multiple devices may be tested in parallel. See col. 7, lines 43-55. There is no indication in the Momohara patent of a hierarchical program structure including a measurement level, a test level and a procedure level as claimed. The program structure disclosed in the Momohara patent is straightforward and serial in nature as evidenced by the flow charts in Figures 14-24b that show various

embodiments of the invention claimed in the Momohara patent with conditional execution of smaller processes based upon the results of earlier measurements. See col. 10, lines 45-53. In order for a reference to anticipate a claim, all elements found in the claim must also be disclosed in the cited reference. The Momhara reference describes a parallel process program structure, but does not describe a hierarchical program structure. Accordingly, the Momohara patent is insufficient to anticipate claim 1 and withdrawal of the rejection is respectfully requested. Allowance of claim 1 is solicited.

Claim 2 is rejected as anticipated by the Momhara patent. Claim 2 remains unamended. Claim 2 depends from claim 1, which is believed to be patentably distinct. Accordingly, for at least the same reasons claim 1 is considered patentable, claim 2 is also believed to be patentably distinct. Figure 9 of the Momohara patent represents the relationships between the total test time for one wafer and the memory capacity. See col. 7, lines 35-37. Figure 9 does not represent or disclose anything related to "a datapoint level corresponding to a single result of a measurement and the measurement level includes a plurality of said

datapoints" as claimed. Accordingly, the Momhara patent is insufficient to anticipate claim 2 and withdrawal of the rejection is respectfully requested. Allowance is solicited.

Claim 3 is rejected as anticipated by the Momohara patent. In response, claim 3 remains unamended. There is no indication in the Momohara patent of a hierarchical program structure including a measurement level, a test level and a procedure level as claimed. Figure 9 of the Momohara patent represents the relationships between the total test time for one wafer and the memory capacity. See col. 7, lines 35-37. Figure 9 does not represent or disclose a measurement level or a test level as part of a hierarchical program structure. Accordingly, the Momohara patent is insufficient to anticipate claim 3 and withdrawal of the rejection is respectfully requested. Allowance is solicited.

Claims 4, 5, and 8-10 are rejected as anticipated by the Momhara patent. Claims 4, 5, and 8-10 remain unamended. Claim 4, 5, and 8-10 depend from claim 3, which is believed to be patentably distinct. Accordingly, for at least the same reasons claim 3 is considered patentable, claims 4, 5, and 8-10 are also believed to be patentably distinct. Allowance is solicited.

Applicant acknowledges objection to claims 6 and 7 as depending upon a rejected base claim, but would be allowable if rewritten in independent form.

Claim 11 is rejected as anticipated by the Momohara patent. In response, claim 11 remains unamended. The Momohara patent proposes to decrease the overall device test time by separating a semiconductor test into two parts, where one part may be executed in parallel with execution of the other part. See col. 4, lines 36-54. Specifically, the time for analyzing the redundancy of the device overlaps with the testing time of the DC characteristic of the same device. See col. 4, lines 55-59. Claim 11, by contrast, recites a "hierarchical structure having multiple levels, each level embodied in the electronics test system as a function defined by a class…including a measurement class…a test class…and a procedure class". The Momohara patent does not disclose a hierarchical structure, nor does it propose to embody a function defined by a class. Accordingly, the Momohara patent is insufficient to anticipate claim 11 and withdrawal of the rejection is respectfully requested. Allowance is solicited.

Applicant acknowledges objection to claims 12, 13, 15, 17, 19 and 20 as depending upon a rejected

base claim, but would be allowable if rewritten in independent form.

Claims 14, 16 and 18 are rejected as anticipated by the Momohara patent. Claims 14, 16 and 18 remain unamended. Claims 14, 16 and 18 depend from claim 11, which is believed to be patentably distinct. Accordingly, for at least the same reasons claim 11 is considered patentable, claims 14, 16 and 18 are also believed to be patentably distinct. In addition, the Momohara patent discloses a memory tester component structure (Figure 8), a relationships between the total test time for one wafer and the memory capacity (Figure 9 and col. 7, lines 35-37, and separation of two processes used to test one device that may be performed in parallel (Figure 14). The Momohara patent does not describe a hierarchical program structure with the specific limitations claimed. Accordingly, withdrawal of the rejection is respectfully requested and allowance is solicited.

Claim 21 is rejected as anticipated by the Momohara patent. In response, claim 21 remains unamended. Figure 9 of the Momohara patent shows the relationships between the total test time for one wafer and memory capacity. See col. 7, lines 35-37. Figure 8 of the Momohara patent discloses a

component level diagram of a semiconductor tester where item 150 represents the test station where a wafer may be probed to provide electrical access to the device under test. See col. 6, lines 28-31. Figure 15 of the Momohara patent discloses an embodiment of a test process wherein two parts of the test of the device are executed in parallel. None of the cited Figures describe a set of functions wherein the implementation of the function is defined by a hierarchical structure, implementing the functions to define test system software program, generating the test system software objects by implementing the functions, and utilizing the software objects to test the DUT. Accordingly, the Momohara patent is insufficient to anticipate claim 21 and withdrawal of the rejection is respectfully requested. Allowance is solicited.

Applicant acknowledges objection to claim 22 as depending upon a rejected base claim, but would be allowable if rewritten in independent form.

Claim 23 is rejected as anticipated by the Momohara patent. In response, claim 23 remains unamended. Figure 9 represents the relationships between the total test time for one wafer and memory capacity. See col. 7, lines 35-37. The Momohara patent does not describe the use of measurement

objects corresponding to a measurement to be performed on a device and a test software object defining a test algorithm utilizing parameters provided by said measurement object and corresponding to a test to be performed on the device. The Momohara patent proposes to separate a semiconductor test into two parts, one part being capable of parallel execution with the other part, for the purpose of reducing overall test time. See col. 4, lines 36-54. The parallel execution disclosed in the Momohara patent is not a hierarchical structure as claimed. Accordingly, the Momohara patent is insufficient to anticipate claim 23 and withdrawal of the rejection is respectfully requested. Allowance is solicited.

Applicant acknowledges objection to claim 24 as depending upon a rejected base claim, but would be allowable if rewritten in independent form.

Claims 25 and 27 remains cancelled. Claim 26 is cancelled.

If any clarifications can be made by way of telephonic interview, the Examiner is invited to contact the Undersigned.

Respectfully submitted,
Christopher Sutton
Applicant

June L. Bouscaren
Patent Attorney
Registration No. 37,928
Attorney for Applicants
Phone: (970) 206-9177